Remarks

Applicants respectfully request reconsideration of this application as amended. Claim 11 has been amended. No claims have been cancelled. Therefore, claims 1-24 are presented for examination.

Claims 1-4, 11-12, 14-16 and 19-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kelleher (U.S. Patent No. 5,287,438) in view of Huang et al. (U.S. Patent No. 5,682,522). Applicants submit that the present claims are patentable over Kelleher in view of Huang.

Kelleher discloses a system for drawing a triangle in aliased form. The system includes a CPU coupled to a floating point processor (FPU). The CPU is also coupled to a random access memory (RAM), a cache and an interface in a graphics subsystem via a 32-bit system bus. The interface is coupled to a graphics processor within the subsystem. The graphics processor is coupled to a frame buffer. The frame buffer is connected to a video digital to analog converter (DAC). The DAC is connected to video display. The graphics processor uses super-sampling to combat the effects of aliasing. See Kelleher at Fig.2 and Abstract. Nevertheless, Kelleher does not disclose or suggest a processor having a CPU core and a graphics core.

Huang discloses a shared memory architecture of graphics frame buffer and hard disk cache. The architecture includes a system bus interface, a hard disk controller, a graphics controller, an arbiter, a memory and a shared memory block. The shared memory block is divided into graphics frame buffer memory and hard disk controller cache memory. The arbiter determines the shared memory access priority between the graphics controller and the hard disk controller. By means of hardware implementation, the graphics controller and the disk controller can share memories. See Huang at Fig. 2 and Abstract. However, Huang does not disclose or suggest a processor having a CPU core and a graphics core.

Claim 1 of the present application recites a processor including a CPU core to execute non-graphic instructions, a graphics core to compute graphical transformations via supersampling techniques and a unified graphics cache coupled to the graphics core to store a supersampled image. As discussed above, neither Kelleher nor Huang disclose or suggest a processor having a CPU core and a graphics core. Instead, Kelleher discloses a CPU and a separate graphics subsystem having a graphics processor. Thus, Kelleher does not disclose that the CPU and the graphics processor are included within a processor. Since neither Kelleher nor Huang disclose or suggest a processor having a CPU core and a graphics core, any combination of Kelleher and Huang would also not disclose or suggest such a feature. Accordingly, claim 1 is patentable over Kelleher in view of Huang.

Claims 2-10 depend from claim 1 and include additional limitations. Thus, claims 2-10 are also patentable over Kelleher in view of Huang.

Claim 11 recites receiving polygons of a first tile of the image at a graphics core, amplifying the polygons at the graphics core and rendering the polygons of the first tile into a unified graphics cache. Applicants submit that nowhere in Kelleher or Huang is there disclosed a method that includes amplifying polygons at a graphics core and rendering the polygons of into a unified graphics cache. Since neither Kelleher nor Huang disclose or suggest such a feature, any combination of Kelleher and Huang would also not disclose or suggest the feature. As a result, claim 11 is patentable over Kelleher in view of Huang. Because claims 12-19 depend from claim 11 and include additional limitations, claims 12-19 are also patentable over Kelleher in view of Huang.

Claim 20 recites a CPU comprising a CPU core to execute non-graphic instructions and a graphics accelerator to compute graphical transformations via supersampling techniques. Thus, for the reasons described above with respect to claim 1, claim 20 is also patentable over Kelleher in view of Huang. Since claims 21-24 depend from claim 11 and include additional limitations, claims 21-24 are also patentable over Kelleher in view of Huang.

Claims 9, 13 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kelleher in view of Huang as applied to claims 1-8, 10-12 and 14-16, and further in view of Pfister et al. (U.S. Patent No. 6,448,968). Applicants submit that the present claims are patentable over Kelleher and Huang even in view of Pfister.

Pfister discloses a method for modeling a representation of a graphic object. A surface of the object is partitioned into a plurality of cells having a grid resolution related to an image plane resolution. A single zero-dimensional surface element is stored in the memory for each cell located on the surface of the object. The surface elements in adjacent cells are connected by links, and attributes of the portion of the object contained in the cell are assigned to each surface element and each link. The location of the attributed surface elements can be moved according to forces acting on the object. See Pfister at Abstract.

However, Pfister does not disclose or suggest a processor having a CPU core and a graphics core. In addition, Pfister does not disclose or suggest receiving polygons of a first tile of the image at a graphics core, amplifying the polygons at the graphics core and rendering the polygons of the first tile into a unified graphics cache. As described above, Kelleher and Huang also do not disclose or suggest such features. Accordingly, any combination of Kelleher, Huang and Pfister would also not disclose or suggest a processor having a CPU core and a graphics core, or receiving polygons of a first tile of the image at a graphics core, amplifying the polygons at the graphics core and rendering the polygons of the first tile into a unified graphics cache. Thus, the present claims are patentable over Kelleher and Huang in view of Pfister.

Claims 10 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kelleher in view of Huang and Pfister as applied to claims 1-9, and 11-17 above, and further in view of Li et al. (U.S. Patent No. 5,860,060). Applicants submit that the present claims are patentable over Kelleher, Huang and Pfister even in view of Li.

Li discloses a data processing device that uses a portion of random access memory as an output buffer for holding a portion of a stream of PCM data, which is to be output to a

digital to analog converter. D/A forms a left analog channel and a right analog channel for speaker subsystems and. The PCM data stream is stored in the output buffer so that PCM data samples which pertain to the left channel are stored at even address and PCM data samples which pertain to the right channel are stored at odd address. Control circuitry monitors direct memory access (DMA) transfers which transfer PCM data samples to PCM serializer. By comparing the address of each DMA transfer to a left/right channel signal from the D/A, the control circuitry can verify that channel synchronization is correct. If a synchronization error is detected, an channel synchronization error correction procedure is invoked. See Li at Abstract.

Nonetheless, Li does not disclose or suggest a processor having a CPU core and a graphics core, or receiving polygons of a first tile of the image at a graphics core, amplifying the polygons at the graphics core and rendering the polygons of the first tile into a unified graphics cache. As described above, Kelleher, Huang and Pfister also do not disclose or suggest such features. Accordingly, any combination of Kelleher, Huang, Pfister and Li would also not disclose or suggest a processor having a CPU core and a graphics core, or receiving polygons of a first tile of the image at a graphics core, amplifying the polygons at the graphics core and rendering the polygons of the first tile into a unified graphics cache. Thus, the present claims are patentable over Kelleher, Huang and Pfister in view of Li.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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